REMARKS

By this amendment, claim 1 has been amended and claims 5-15 have been cancelled in the application. Currently, claims 1-4 are pending in the application.

The indication that claims 2-4 are allowed is noted with appreciation.

Claim 1 was rejected under 35 USC 102(b) as being anticipated by Suzuki et al. (Japanese Patent Application Publication No. 4-291576).

This rejection is respectfully traversed in view of the amendments to claim 1 and the remarks below.

The present invention relates to a solid state imaging device having a timing signal generation circuit and a clamping circuit.

The present invention discloses that Fig. 9 is a block diagram showing the structure of the OB clamping circuit 3. An amplifier 12 corresponds to the first amplifier means and an amplifier 11 corresponds to the second amplifier. A switch 14 and a capacitor C3, which is a retention section, correspond to the sampling means (see page 13, lines 12-20). A target value setting circuit 10 is a device which sets a target value α for the output of the amplifier 11, and normally is a variable resistor or the

like which divides the voltage ±Vcc of the power source (see page 14, lines 2-5).

The present invention also discloses that Fig. 10 is a timing chart for this first preferred embodiment during n-field accumulation, while Fig. 11 is a version thereof with the amplitude enlarged. The CCD 1 outputs for just one vertical period, and the signal OBCP 6 also operates in the vertical period, and steps during the period S. In the period T, the signal OBCP 6 goes to ON at a timing of each individual horizontal period, and the signal which has been inputted to the capacitor C3 is fed back via the amplifiers 11 and 12. Accordingly the voltage of the capacitor C3 during the period T3 varies around some constant value as a center, while during the period S its last value is maintained. In the period S the switch 14 goes to the open state, and the feedback signal is no longer obtained.

On the other hand, the enable signal 7 is supplied from the timing signal generation circuit 5 to the switches 15 and 16, so that their ON/OFF is controlled. As shown in Fig. 10, during the period T the enable signal 7 goes to the H level, while during the period S it goes to the L level. During the period T in which the enable signal 7 is at the H level, the switch 15 is in the ON state (closed), while the switch 16 is in the OFF state (open),

and the output value of the amplifier 11 is inputted to the capacitor C2. Accordingly it never happens that the switches 14 and 16 are ON at the same time. In the period S in which the enable signal 7 is at the L level, the switch 15 is OFF, and the average value of the output of the amplifier 11 is maintained in the capacitor C2, while the switch 16 is in the ON state. The output of the capacitor C2 and the output of the amplifier 11 are inputted to the amplifier 13, and the difference thereof is amplified therein and is supplied to the capacitor C3. As a result if this, the output of the amplifier 11 is altered by the operation of the feedback control (see page 14, line 20 - page 6, line 4).

By this amendment, claim 1 has been amended to include some of the features similar to claim 2. Specifically, claim 1 recites "a clamping means, comprising a first amplifier means for inputting the output of said solid state imaging element at one of the input terminals; a sampling means for sampling the output of said first amplifier means and which includes a switch which goes ON during said optical black section and a retention section; a target value setting means which sets a target value for output; and a second amplifier means for receiving the output from said first sampling means and said target value level from said target

value setting means via a low pass filter means, amplifying the difference between them, and inputting the difference to said first amplifier means; which amplifies the difference between the output of said second amplifier means when the enable signal is active and retains the output of said second amplifier means when the enable signal is inactive, and feeds back the amplified signal to said first sampling means during a period said enable signal is active". These features are not shown on suggested by Suzuki et al.

Suzuki et al. relates to a clamp circuit for electron endoscope device to enable satisfactory gamma correction processing by matching the blank part of the video signal to the black level of the black part in the clamp circuit.

Suzuki et al. disclose the clamping circuit that receives a signal Clamp pulse and CBLK (see Figs. 3 and 6).

Suzuki et al. do not disclose a clamping means, comprising a first amplifier means for inputting the output of the solid state imaging element at one of the input terminals; a sampling means for sampling the output of the first amplifier means and which includes a switch which goes ON during the optical black section and a retention section; a target value setting means which sets a target value for output; and a second amplifier means for

receiving the output from the first sampling means and the target value level from the target value setting means via a low pass filter means, amplifying the difference between them, and inputting the difference to the first amplifier means; which amplifies the difference between the output of the second amplifier means when the enable signal is active and retains the output of the second amplifier means when the enable signal is inactive, and feeds back the amplified signal to the first sampling means during a period the enable signal is active as claimed in claim 1.

Applicants respectfully submit that the blanking pulse, or the CBLK, of Suzuki is clearly different from the enable signal of the present invention. The enable pulse is active once during one of a number of vertical periods when CCD outputs the image signal as shown in Fig. 10. However, the blanking signal of Suzuki et al. becomes active once every period (H). Therefore, applicants respectfully submit that the blanking signal of Suzuki et al. is completely different from the enable signal of the present invention.

Also, applicants respectfully submit that Suzuki et al. do not disclose the clamp circuit amplifies the difference between the output of the second amplifier when the enable signal is

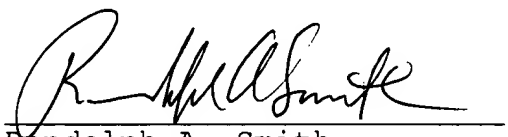
active and retains the output of the second amplifier when the enable signal is inactive. According to the present invention, shading or oscillatory phenomena can be prevented even when charge is accumulated in the solid state imaging elements by a plurality of fields.

For these reasons, it is believed that Suzuki et al. do not show or suggest the present claimed features of the present invention. It is therefore submitted that independent claim 1 is allowable over Suzuki et al.

In view of foregoing claim amendments and remarks, it is respectfully submitted that the application is now in condition for allowance and an action to this effect is respectfully requested.

If there are any questions or concerns regarding the amendments or these remarks, the Examiner is requested to telephone the undersigned at the telephone number listed below.

Respectfully submitted,



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